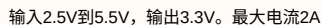
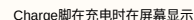
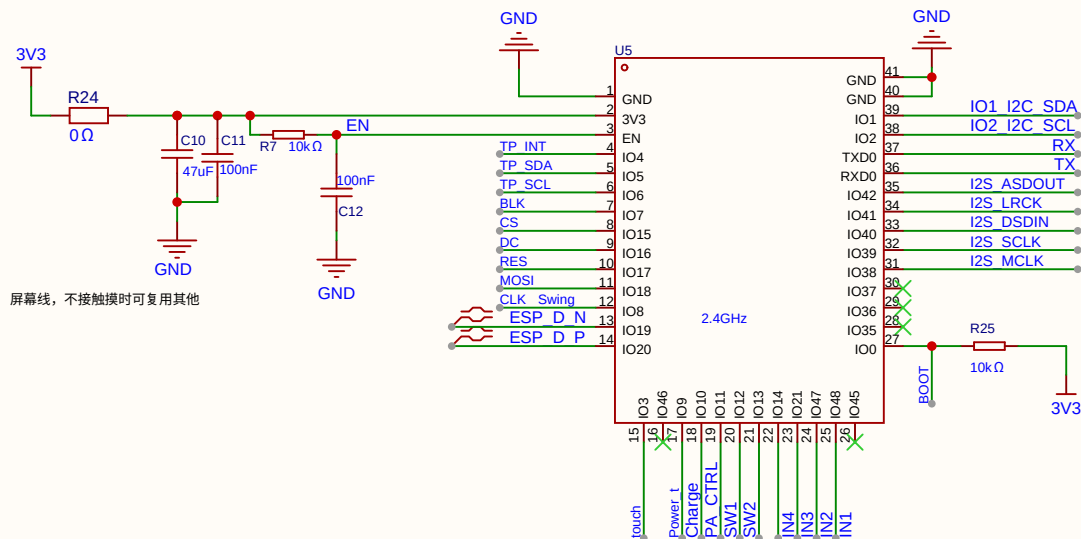


2代板的基础上进行接口优化及功能优化

- 1、电机接口换间距2.54
- 2、烧录口换间距2.54
- 3、预留针脚优化、磁线圈方案优化
- 4、屏幕接口优化
- 5、电源模块不需要5v升压
- 6、功放倍率调整

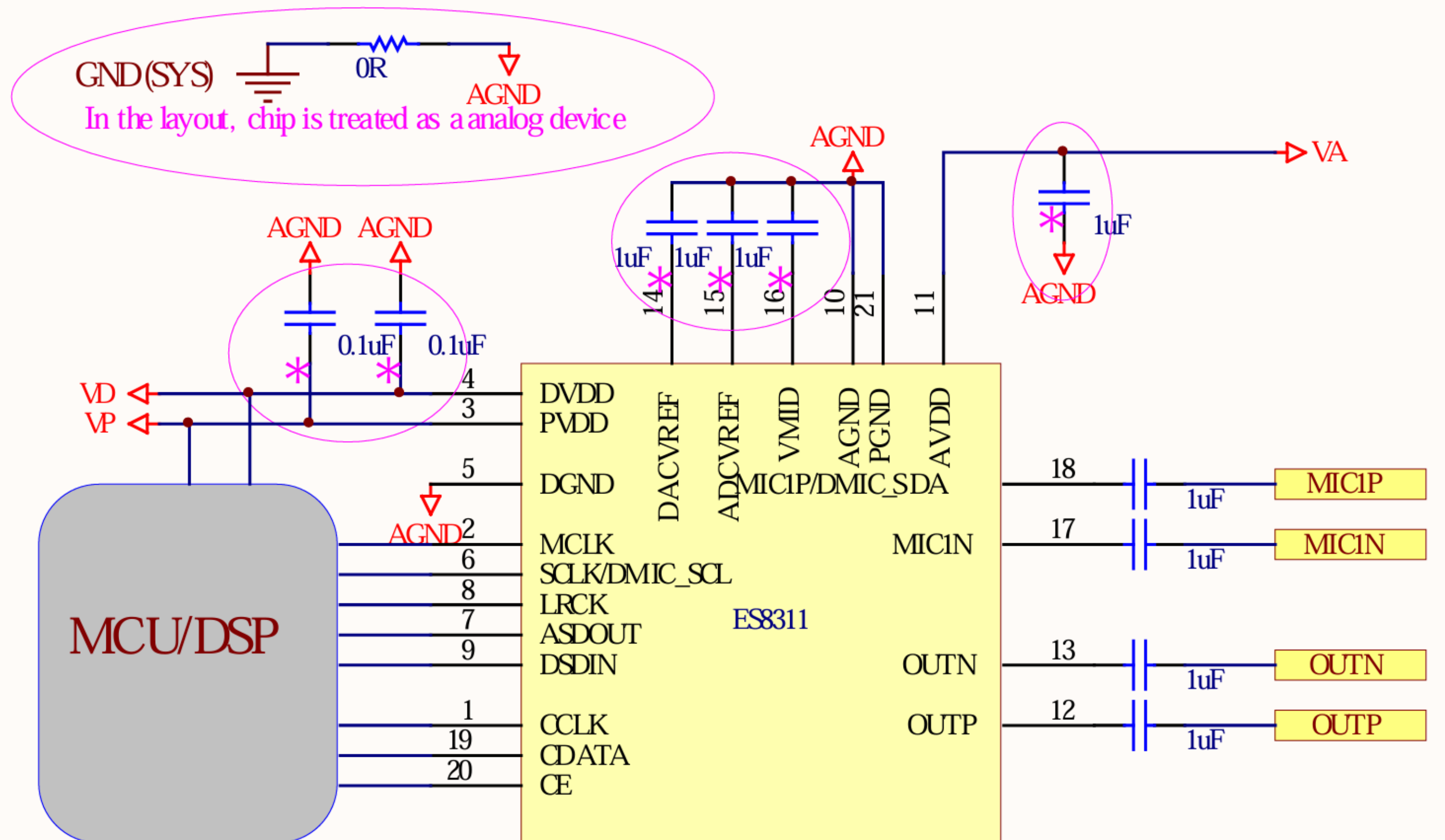
原理图	招财猫0.3&商界0.2		创建日期	2026-07-14
			更新日期	2026-07-14
板子	招财猫0.3&商界少年		图页	P1
绘制		LuckyCat&商界少年		
审阅				
		版本	尺寸	页 1 共 6
嘉立创EDA		V1.0	A4	嘉立创EDA





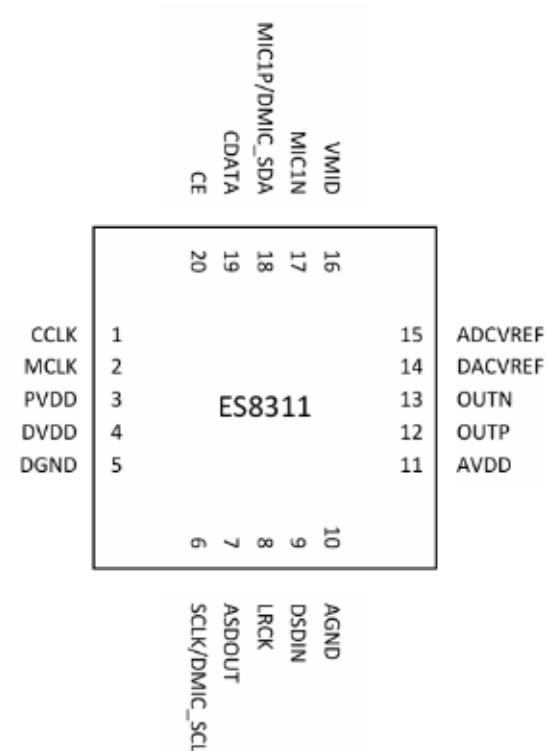
原理图	招财猫0.3&商界0.2			创建日期	2026-07-20
				更新日期	2026-07-20
板子	招财猫0.3&商界少年			图页	MCU
绘制		LuckyCat&商界少年			
审阅					
		版本	尺寸	页 3 共 6	
		V1.0	A4	嘉立创EDA	

3. TYPICAL APPLICATION CIRCUIT

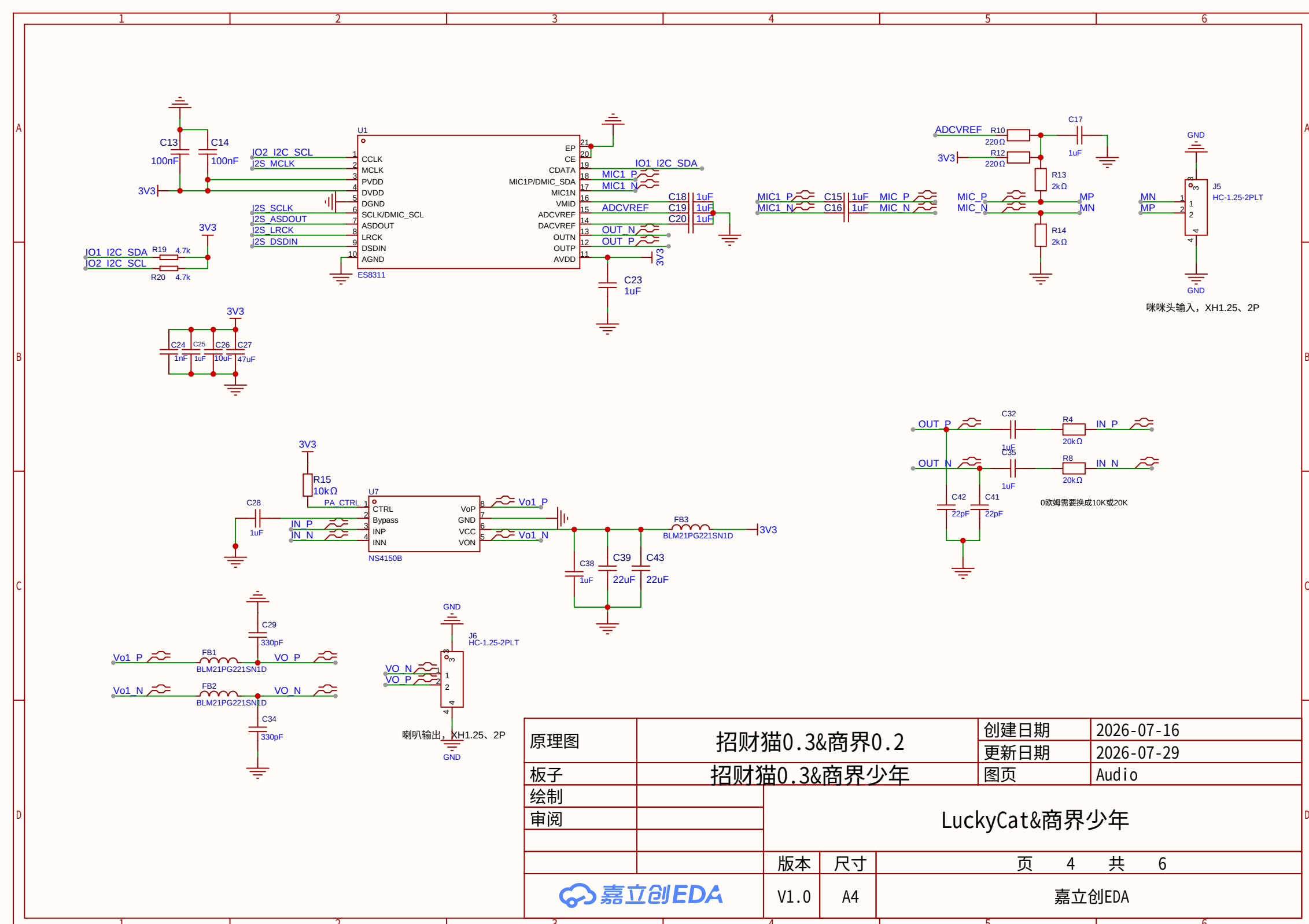


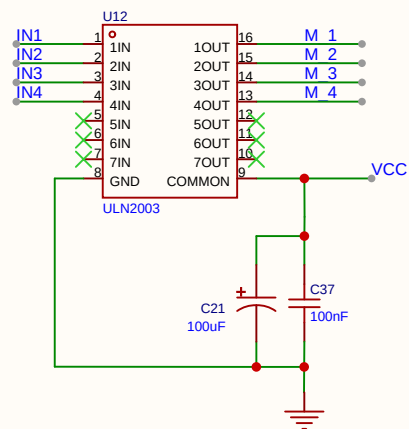
For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible
* Additional paralle capacitors(typically 0.1 μ F) can be used, larger value capacitors(typically 10 μ F) would also help

2. PIN OUT AND DESCRIPTION

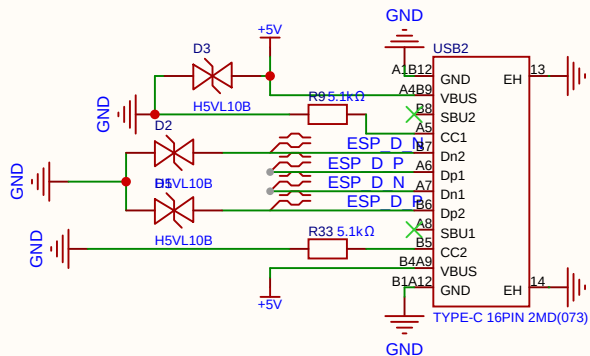


Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATE, CE	1, 19, 20	I, I/O, I	I ² C clock, data, address
MCLK	2	I	Master clock
SCLK/DMIC_SCL	6	I/O	Serial data bit clock/DMIC bit clock
LRCK	8	I/O	Serial data left and right channel frame clock
ASDOUT	7	O	ADC serial data output
DSDIN	9	I	DAC serial data input
MIC1P/DMIC_SDA	18	I	Mic input
MIC1N	17	I	Mic input
OUTP, OUTN	12, 13	O	Differential analog output
PVDD	3	Analog	Power supply for the digital input and output
DVDD, DGND	4, 5	Analog	Digital power supply
AVDD, AGND	11, 10	Analog	Analog power supply
VMID	16	Analog	Filtering capacitor connection
ADCVREF, DACVREF	15, 14	Analog	Filtering capacitor connection

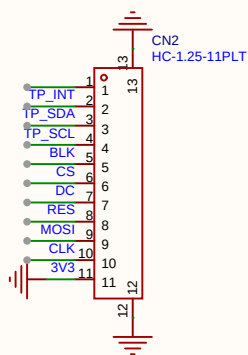




原理图	招财猫0.3&商界0.2		创建日期	2026-07-16
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绘制			LuckyCat&商界少年	
审阅				
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嘉立创EDA		V1.0	A4	嘉立创EDA

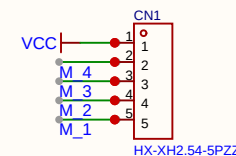
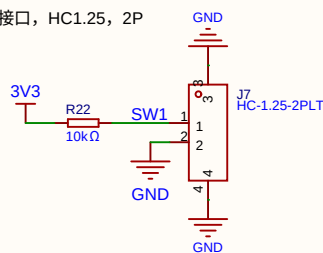


USB接口无变化

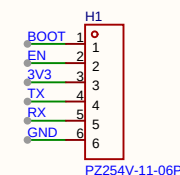


屏幕接口

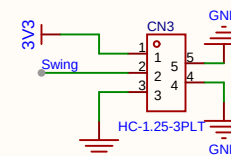
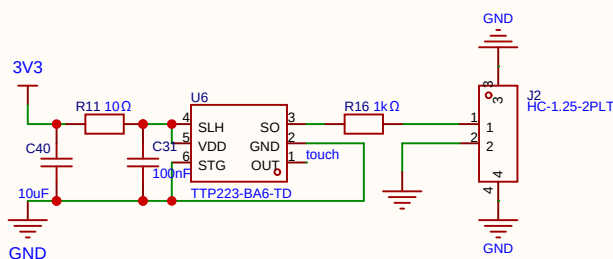
微动开关接口, HC1.25, 2P



步进电机接口



烧录口



原理图	招财猫0.3&商界0.2		创建日期	2026-07-17
板子	招财猫0.3&商界少年		更新日期	2026-07-29
绘制			图页	Connectors
审阅			LuckyCat&商界少年	
			版本	尺寸
			页	6 共 6
嘉立创EDA		V1.0	A4	嘉立创EDA